## REMARKS

Reconsideration of the present application is respectfully requested. Claims 5-8 and 12 are rejected as failing to comply with the enablement requirement of 35 U.S.C. §112, ¶ 1. Claims 1 and 3-12 are rejected as failing to comply with the written description requirement set forth in the paragraph 1 of section 112. Claims 1, 5, 8-9, and 11 are rejected under 35 U.S.C. §102(b) as anticipated by JP10-227184. Claims 3, 6-7 and 10 are rejected under 35 U.S.C. §103(a) as unpatentable over JP '184 in view of Hunter U.S. Patent No. 6,697,517.

Concerning the rejection pursuant to 35 U.S.C. §112, ¶ 1, for failure to provide an enabling disclosure, it is observed that the basis for rejection is not complete. Accordingly, a *prima facie* case for a non-enabling disclosure has not been set out. The test here for determining enablement is succinctly set forth in §2164.01 of the MPEP, where it is said,

> Any analysis of whether a particular claim is supported by the disclosure in an application requires a determination of whether that disclosure, when filed, contained sufficient information regarding the subject matter of the claims as to enable one skilled in the pertinent art to make and use the claimed invention. The standard for determining whether the specification meets the enablement requirement was cast in the Supreme Court decision of *Mineral Separation v. Hyde*, 242 U.S. 261, 270 (1916) which postured the question: is the experimentation needed to practice the invention undue or unreasonable? That standard is still the one to be applied. *In re Wands,* 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988). Accordingly, even though the statute does not use the term 'undue experimentation,' it has been interpreted to require that the claimed invention be enabled so that any person skilled in the art can make and use the invention without undue experimentation. *In re Wands*, 858 F.2d at 737, 8 USPQ2d at 1404 (Fed. Cir. 1988). See also *United States v. Telectronics, Inc.*, 857 F.2d 778, 785, 8 USPQ2d 1217, 1223 (Fed. Cir. 1988) ('The test of enablement is whether one reasonably skilled in the art could make or use the invention from the disclosures in the patent coupled with information known in the art without undue experimentation.'). A patent need not teach, and preferably omits, what is well known in the art. *In re Buchner,* 929 F.2d 660, 661, 18 USPQ2d 1331, 1332 (Fed. Cir. 1991); *Hybritech, Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1384, 231 USPQ 81, 94 (Fed. Cir. 1986), *cert. denied*, 480 U.S. 947 (1987); and *Lindemann Maschinenfabrik GMBH v. American Hoist*

*& Derrick Co.*, 730 F.2d 1452, 1463, 221 USPQ 481, 489 (Fed. Cir. 1984). Determining enablement is a question of law based on underlying factual findings. *In re Vaeck*, 947 F.2d 488, 495, 20 USPQ2d 1438, 1444 (Fed. Cir. 1991); *Atlas Powder Co. v. E.I. du Pont de Nemours & Co.*, 750 F.2d 1569, 1576, 224 USPQ 409, 413 (Fed. Cir. 1984).

Upon review of the rejection and basis therefore, it is submitted that there is no contention that the invention of claims 5-8 and 12 are not enabled because, to arrive at the claimed subject matter that the experimentations need to practice the invention, is undue. Accordingly, since the necessary showing has not been made here, the rejection cannot stand as presently advocated. Moreover, it is further noted that if one considers the factors to be applied in considering whether the level of experimentation necessary is "undue", the factors mitigate clearly in favor of the applicant[1]. The claims at issue are dependent claims, and are not of exceptional breadth. The level of skill in the art is relatively high. Furthermore, with regard to prior art, it is observed that claims 5-8 are rejected under 35 U.S.C. §102(b) or §103(a). It is submitted that it is inconsistent for the examiner to, one the one hand, argue that these claims are not enabled, yet then argue that the prior art teaches these same claims[2]. At the least, he undercuts his lack of enablement argument by citing prior art believed to teach the invention. For these reasons, it is submitted that the enablement rejection under 35 U.S.C. §112, ¶ 1is traversed.

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[1] These factors are set forth in MPEP § 2126.01 (a) and include, but are not limited to:

(A) The breadth of the claims;
(B) The nature of the invention;
(C) The state of the prior art;
(D) The level of one of ordinary skill;
(E) The level of predictability in the art;
(F) The amount of direction provided by the inventor;
(G) The existence of working examples; and
(H) The quantity of experimentation needed to make or use the invention based on the contact of the disclosure.

*In re Wands*, 858 F.2d 731, 737, 8 USPQ2d 1400, 1404 (Fed. Cir. 1988).

[2] The applicant in no way admits to unpatentability under any of the grounds advocated by the examiner in the present office action. They merely wish to point out that the examiner's argument with respect to enablement is fatally inconsistent.

Claims 1 and 3-12 are rejected as failing to comply with the written description requirement set forth in the 35 U.S.C. §112, ¶ 1. The claims are so rejected because the examiner contends that the applicants did not possess, at the filing date, an invention including the emboldened limitation of claim 1:

> "recognition processing means for performing recognition processing including calculation of an evaluation score representing a read likelihood ratio for an image output from said image sensing optical means for every read optical condition, and for adopting a recognition result for the character string exhibiting the highest score as an ID of the semiconductor wafer under the read optical condition, **the highest score being adopted only if it is at least equal to a predetermined minimum score**"

Upon a review of the specification, it is not understood how this rejection can be sustained. The written description of the present invention describes the structure as including what is need to perform this task, namely that the semiconductor wafer ID recognition apparatus of the preferred embodiments include

> read optical condition memories, (to be referred to as condition memories hereinafter) 5-1 to 5-5 for storing a plurality of read optical conditions, a plurality of ID recognition processors 6-1 to 6-5 for performing ID recognition processing by using an output from the image sensing optical section 1b under respective read optical conditions, a score comparator 7 for comparing evaluation scores stored in the ID recognition processors 6-1 to 6-5, a wafer ID input unit 8 for manually inputting an ID when no ID can be recognized by automatic read under a plurality of read optical conditions registered in advance, a wafer ID determination processor 9 for determining, as the ID of a semiconductor wafer, a recognition result under a read optical condition exhibiting the highest evaluation score. See specification at page 5 line 17 – page 6 line 5.

The present specification further discloses that the ID recognition processors are capable of performing the task at the center of the present controversy. It is indicated that:

> As shown in Fig. 1C, each of the ID recognition processors 6-1 to 6-5 has a recognition unit 6a for performing recognition processing for respective images obtained under a plurality of read optical conditions, an evaluation unit 6b for calculating an evaluation score representing a read likelihood ratio for each read optical condition on the basis of the recognition result of the recognition unit 6a, and a memory 6c for storing the recognition result and evaluation score. Specification at page 6 lines 11-20

Now with the structures and capabilities of the present invention demonstrated above, it can now be shown that the applicant possessed the claimed invention at the time of filing. The claimed step of at issued here, that is,

> "the highest score being adopted only if it is equal to a predetermined minimum score"

is directly supported in the specification at p. 7 of the specification, where it is disclosed that,

> "More specifically, the wafer ID recognition sorter 1 repetitively inspects an ID under a plurality of read optical conditions registered in advance, and compares evaluation scores each representing a read likelihood ratio under each read optical condition at the last of inspection. *The wafer ID recognition sorter 1 recognizes, as the ID of the wafer, a read result having the highest score equal to or higher than an arbitrarily set acceptable score (reference score).*" Specification at page 7 lines 16-24 (Emphasis added).

It is submitted that the above specification excerpt conclusively demonstrates that applicants possessed the invention of claim 1 at the time the invention was made.

Claims 1, 5, 8, 9 and 11 are rejected under 35 U.S.C. § 102 (b) as allegedly being anticipated by Ono Satoru, Japanese Patent Publication No. 2000-055820 (JP Application No. 10-227184). This rejection is traversed.

In rejecting claim 1 the Examiner restates the limitations of this claim and then draws the reader's attention to the portions of a translation of Ono Satoru which purport to teach such limitations. With respect to the limitations of claim 1 discussed above which recites that

> "recognition processing means for performing recognition processing including calculation of an evaluation score representing a read likelihood ratio for an

image output from said image sensing optical means for every read optical condition, and for adopting a recognition result for the character string exhibiting the highest score as an ID of the semiconductor wafer under the read optical condition, **the highest score being adopted only if it is at least equal to a predetermined minimum score**"

The examiner draws the applicant's attention to paragraphs 0016 and 0017 of Onu Satoro. As read by applicant, it seems that what is disclosed in this paragraph is the selection of the character string of the examiner wafer (Z6W4), as opposed to the adoption of a score "only if it is at least equal to a predetermined score." Accordingly, Onu Satoro does not anticipate the claimed invention, and in fact teaches away from same.

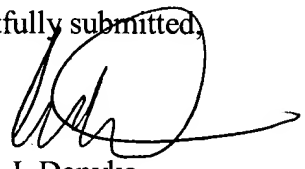
Therefore, Ono does not disclose the recitations of independent claim 1. Claims 2, 5, 8, 9, and 11 depend from independent claim 1 and therefore incorporate novel and nonobvious features thereof. Accordingly, claims 2, 5, 8, 9, and 11 are patentably distinguishable over the prior art for at least the reasons that independent claim 1 is patentably distinguishable over the prior art. Therefore, this rejection should now be withdrawn.

***Rejection of Claims 3,6-7 and 10 under 35 U.S.C. § 103***

Claims 3, 6-7 and 10 are rejected under 35 U.S.C. § 103 as allegedly being obvious from Ono Satoru in view of Hunter, U.S. patent No. 6, 697,517. This rejection is traversed. Hunter does not cure the deficiencies of Ono Satoru as they relate to independent claim 1 from which rejected claims 3, 6-7 and 10 depend. Therefore, claims 3, 6-7 and 10 are patentably distinguishable over the prior art for at least the reasons that claim 1 is patentably distinguishable over the prior art.

Wherefore, based upon the foregoing, it is submitted that the application is in condition of allowance and a relatively early reply to this paper would be appreciated.

Respectfully submitted,



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